Remarks

Reconsideration of this Application is respectfully requested.

Status of Claims

Upon entry of the foregoing amendments, claims 8-12, 14-18 and 20-81 are pending in the application, with claims 8, 14, 30, 36, 38, 41, 43 and 63 being the independent claims. Claims 1-7, 13 and 19 were previously canceled. Claim 30 is amended. Claims 43-81 are added. These changes are believed to introduce no new matter and their entry is respectfully requested.

Applicants thank the Examiner for indicating that claims 20-24 and 39 are allowable.

Based on the foregoing amendments and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Information Disclosure Statement

Applicants confirm that they filed an Information Disclosure Statement (IDS) on March 24, 2004, citing (among other documents) U.S. Patent No. 4,901,233 to Liptay, U.S. Patent No. 5,134,561 to Liptay, and U.S. Patent No. 5,473,764 to Chi. A second IDS also filed on March 24, 2004 — which cites U.S. Patent No. 4,879,787 to Walls — has been mistakenly included in the prosecution history of the instant application. Applicants respectfully request that this second IDS be removed.

Initial Matters

On January 25, 2007, a final Office Action ("the January 25th Office Action") issued in the instant case. In response, Applicants filed an Amendment and Reply on May 25, 2007 ("the May 25th Amendment and Reply"). On June 8, 2007, an Advisory Action was mailed, indicating that the May 25th Amendment and Reply would not be entered. In response, Applicants filed a Request for Continued Examination (RCE), a Petition for Extension of Time, and the corresponding fees on June 19, 2007. Thus, the May 25th Amendment and Reply was timely filed with the appropriate fees.

The arguments set forth in the May 25th Amendment and Reply should have been entered and considered. *See* 37 C.F.R. § 1.114(d) ("If an applicant timely files a submission and fee set forth in § 1.17(e), the Office will withdraw the finality of any Office action and the submission will be entered ***and considered.***") (emphasis added); 37 C.F.R. § 1.114(c) (stating that a submission includes new arguments). Although the finality of the January 25th Office Action has been withdrawn, the Office Action of September 6, 2007 ("the instant Office Action") does not include any discussion regarding the arguments set forth in the May 25th Amendment and Reply. Thus, it appears that the Examiner has not considered all the arguments Applicants previously presented.

Accordingly, arguments previously presented are incorporated by reference and expanded upon herein. Applicants respectfully request that all these arguments be entered and considered.

Rejections under 35 U.S.C. § 103

Claims 8-12, 14-18, and 25-29

Claims 8-12, 14-18 and 25-29 were rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U.S. Patent No. 5,488,729 to Vegesna *et al.* ("Vegesna") in view of U.S. Patent No. 5,481,734 to Yoshida ("Yoshida"). Applicants respectfully traverse.

Vegesna and Yoshida, alone or in combination, do not teach or suggest each and every feature of independent claim 8. For example, neither Vegesna nor Yoshida teach or suggest "a register rename circuit configured to provide references to locations in the register file for logical register references included with the plurality of buffered instructions," as recited in claim 8.

The Examiner does not contend that Yoshida teaches or suggests such a register rename circuit. (*See* the instant Office Action p. 3 ¶ i.) Applicants agree. The Examiner, nonetheless, asserts that Vegesna teaches the recited "register rename circuit." In support of this assertion, the Examiner cites column 13, lines 50-62 of Vegesna. Upon close review of this portion of Vegesna, however, Applicants cannot find any teaching or suggestion encompassing the recited "register rename circuit."

Column 13, lines 50-62 describe an "approach to dynamic scheduling in the context of parallel floating-point execution units." According to this approach,

> the functional units receive their dependent operands ***straight from the functional units*** which have generated them; the operands are forwarded directly ***rather than waiting for them to be stored first in the register file***, then accessing them from there.

Vegesna col. 13 ll. 57-62 (emphasis added). Because this section of Vegesna expressly teaches that the operands are not even stored in the register file, it does not teach a register rename circuit to provide references to locations in the register file. Thus, Vegesna does not teach or even suggest "a register rename circuit configured to ***provide references to locations in the register file*** for logical register references included with the plurality of buffered instructions," as recited in claim 8 (emphasis added).

In addition, neither Vegesna nor Yoshida teach or suggest, for example, "a branch prediction circuit configured to provide a branch bias signal indicating whether a conditional branch controlled by a conditional branch instruction is predicted to be taken or not taken," as recited in claim 8. The Examiner does not contend that Yoshida teaches or suggests such a branch prediction circuit. (*See* the instant Office Action p. 3 ¶ j.) Applicants agree. The Examiner, nonetheless, asserts that Vegesna teaches the recited "branch prediction circuit," despite Applicants' argument in the May 25th Amendment and Reply to the contrary. That argument is repeated and expanded upon herein. Applicants respectfully request that the Examiner consider this argument.

The plain language of claim 8 recites that the branch bias signal indicates whether a conditional branch controlled by a conditional branch instruction is predicted to be taken or not. The Specification of the instant application describes two different example methods for processing a conditional branch instruction depending on the branch bias signal. (*See* the Specification at ¶¶ [0120]-[0134] ("For 'branch taken bias'"); the Specification at ¶¶ [0135]-[0149] ("For 'branch not taken bias'"). Thus, the branch bias signal enables a microprocessor to handle conditional branch instructions in different manners depending on whether the branch is predicted to be taken or not.

Vegesna does not teach or suggest such a branch bias signal. Although Vegesna appears to disclose a first microprocessor design scheme that always assumes a branch will be taken and a second microprocessor design scheme that always assumes a branch will not be taken (*see* Vegesna col. 10, l. 66 - col. 11, l. 25), Vegesna's architecture is described as being implemented in terms of the SPARC RISC instruction set (*see* Vegesna, col. 17, ll. 61-64), which is a trivial "not-taken" branch prediction design scheme. Because Vegesna's architecture is implemented as a trivial "not-taken" branch prediction design scheme, Vegesna does not teach — and, in fact, simply does not need — a branch bias signal that enables a microprocessor to process a conditional branch instruction by ***either*** assuming the branch will be taken ***or*** assuming the branch will not be taken. Vegesna's architecture simply assumes a branch will not be taken. Thus, Vegesna does not teach or suggest the recited "branch bias signal." Because Vegesna does not even teach a branch bias signal, Vegesna cannot possibly teach or suggest "a branch prediction circuit configured to provide a branch bias signal indicating whether a conditional branch controlled by a conditional branch instruction is predicted to be taken or not taken" — as required by claim 8.

Although it is not necessary for Vegesna and Yoshida to explicitly teach each and every feature of claim 8 (*see Dann v. Johnston*, 425 U.S. 219, 230, 189 USPQ 257, 261 (1976)), the Examiner has failed to even acknowledge any of the above-described differences between claim 8 and the disclosure of Vegesna and Yoshida, as required by controlling Supreme Court precedent. *See Graham v. John Deere Co.*, 383 U.S. 1 (1966) (setting forth required factual inquires for an obviousness-type analysis, including: (1) determining the scope and content of the prior art; (2) ascertaining the differences

between the claimed invention and the prior art; and (3) resolving the level of ordinary skill in the art). Because the Examiner has not even acknowledged any of the above-described differences, the Examiner has *ipso facto* failed to explain how such differences would have been obvious to a person of ordinary skill in the art. Accordingly, the Examiner has failed to establish a *prima facie* case of obviousness of claim 1.

Thus, independent claim 8 is patentable over Vegesna and Yoshida. Independent claim 14 is also patentable over Vegesna and Yoshida for at least the same reasons as independent claim 8 because independent claim 14 recites a method corresponding to the superscalar microprocessor recited in independent claim 8. Dependent claims 9-12, 15-18, and 25-29 are likewise patentable over Vegesna and Yoshida for at least the same reasons as the independent claims from which they depend, and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 8-12, 14-18, and 25-29 be reconsidered and withdrawn.

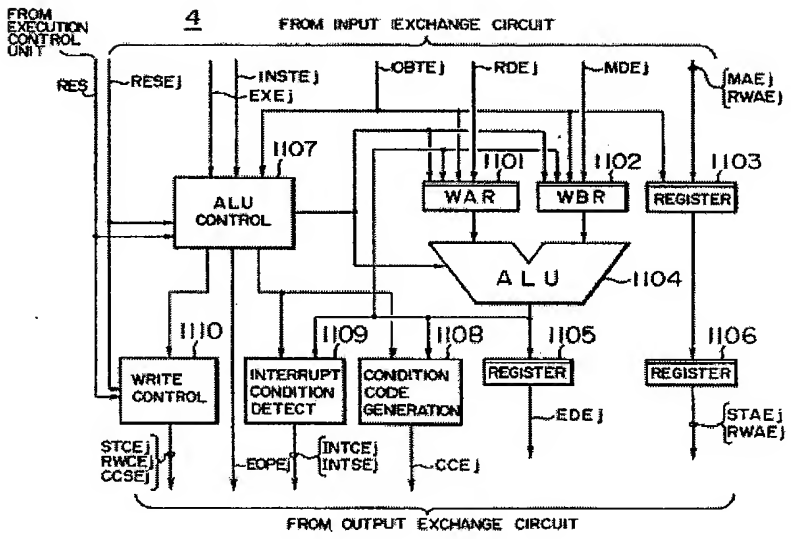
Claims 30-37 and 41

Claims 30-37 and 41 were rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U.S. Patent No. 4,942,525 to Shintani *et al.* ("Shintani") in view of U.S. Patent No. 4,594,655 to Hao *et al.* ("Hao"). Applicants respectfully traverse.

Shintani and Hao, alone or in combination, do not teach or suggest each and every feature of independent claim 30. For example, neither Shintani nor Hao teach or suggest "retiring the instruction group held in the multiple-stage buffer" and "advancing an other instruction group held in the multiple-stage buffer" as currently recited in independent claim 30. The Examiner does not contend that Hao teaches or suggests these features. Applicants agree.

The Examiner, however, asserted that Shintani teaches retirement of instructions. (*See* the Office Action p. 6.) In support of this assertion, the Examiner cites Shintani at column 5, lines 65-68, and column 6, lines 1-7. However, upon close review of these sections, Applicant cannot find any teaching or suggestion directed to retirement of instructions, let alone encompassing the "retiring" and "advancing" features recited in claim 30.

The sections cited by the Examiner are embedded in a discussion of "the j-th execution unit" included in Shintani's architecture. *See* Shintani col. 5 ll. 38-68; col. 6 ll. 1-39; FIG. 11. Referring to FIG. 11 of Shintani (reproduced below), the j-th execution unit includes an arithmetic logic unit (ALU) control circuit 1107, an ALU 1104, and work registers 1101, 1102. According to Shintani, "[t]he ALU control circuit 1107 is a conventional one which comprises a microprogram and an execution control circuit therefor." Shintani col. 5 ll. 62-65. After receiving appropriate control signals, the ALU control circuit 1107 "reads the first microinstruction of the microprogram corresponding to the instruction." Shintani col. 5 ll. 65-68. The ALU then executes the microinstructions in the microprogram. Shintani col. 6 ll. 1-39.



The sections of Shintani cited by the Examiner do not include any discussion of the "retiring" and "advancing" features recited in claim 30. The first section of Shintani cited by the Examiner is column 5, lines 65-68. As set forth above, this section describes how the ALU control circuit 1107 reads the first microinstruction of the microprogram corresponding to an instruction. Column 6, lines 1-7 of Shintani, which were also cited by the Examiner, describe the end of the execution of the microprogram:

> For the instruction whose execution stage completes in one cycle, the end of execution is specified to the first microinstruction, and for the instruction whose execution stage needs a plurality of cycles, the end of execution is specified to the microinstruction which controls the last operation stage, and signal EOPE$_j$ is an output representing the end of execution.

Shintani col. 5 l. 68 - col. 6 ll. 1-7. Thus, these sections of Shintani describe the reading and execution of microinstructions in a microprogram corresponding to an instruction. There is simply no discussion whatsoever in these sections, or in any other section of Shintani, directed to "retiring the instruction group held in the multiple-stage buffer" and

"advancing an other instruction group held in the multiple-stage buffer" as currently recited in independent claim 30.

Because the Examiner has failed to acknowledge the above-described differences between claim 30 and the disclosure of Shintani and Hao, the Examiner has failed to explain how such differences would have been obvious to a person of ordinary skill in the art. Accordingly, the Examiner has failed to establish a *prima facie* case of obviousness of claim 30.

Thus, independent claim 30 is patentable over Shintani and Hao. Dependent claims 31-35 are also patentable over Shintani and Hao for at least the same reasons as independent claim 30 from which they depend, and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 30-35 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Independent claim 36 recites, among other features, "wherein when a plurality of instructions of the instruction group are all retired, an entry in the buffer corresponding to the instruction group is released." As set forth above, neither Shintani nor Hao teach or suggest retirement of instructions. Because these references do not even teach or suggest retirement of instructions, they certainly do not teach or suggest the retirement of instructions as specifically recited in claim 36.

Because the Examiner has failed to acknowledge these differences between claim 36 and the disclosure of Shintani and Hao, the Examiner has failed to explain how such differences would have been obvious to a person of ordinary skill in the art. Accordingly, the Examiner has failed to establish a *prima facie* case of obviousness of claim 36.

Thus, independent claim 36 is patentable over Shintani and Hao. Dependent claim 37 is also patentable over Shintani and Hao for at least the same reasons as independent claim 36 from which it depends, and further in view of its own features. Accordingly, Applicants respectfully request that the rejection of claims 36 and 37 be reconsidered and withdrawn.

Independent claim 41 recites a data processing apparatus comprising a superscalar type microprocessor having a plurality of functional units that can execute instructions simultaneously, wherein the microprocessor includes, among other features:

> an instruction completion unit that advances contents of a plurality of registers of the buffer in the forward direction by a number of stages that correspond to a number of groups of completed instructions.

The Examiner has not cited, and Applicants cannot find, any teaching or suggestion in Shintani or Hao encompassing this claim feature. Because the Examiner has not even acknowledged the differences between claim 41 and the disclosure of Shintani and Hao, the Examiner has failed to explain how such differences would have been obvious to a person of ordinary skill in the art. Accordingly, the Examiner has failed to establish a *prima facie* case of obviousness of claim 41.

Thus, claim 41 is patentable over Shintani and Hao. Accordingly, Applicants respectfully request that the rejection of claim 41 be reconsidered and withdrawn.

Claims 38 and 40

Claims 38 and 40 were rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Shintani in view of Hao, and further in view of U.S. Patent No. 5,237,666 to Suzuki *et al.* ("Suzuki"). Applicants respectfully traverse.

As previously presented, independent claim 38 recites a data processing apparatus comprising a super scalar type microprocessor having a plurality of functional units that can execute instructions simultaneously, wherein the microprocessor includes, among other features:

> a retirement unit that specifies a register in which to store a result of executing the instruction outside the predetermined program order, wherein the retirement unit retires the instruction in program order after the instruction is completed.

As set forth above, neither Shintani nor Hao teach or suggest retirement of instructions. Accordingly, Shintani and Hao do not teach or suggest, for example, the retirement unit recited in claim 38. Furthermore, the Examiner did not cite, and Applicants cannot find, any teaching or suggestion in Suzuki encompassing the retirement unit recited in claim 38.

Because the Examiner has failed to acknowledge the above-described differences between claim 38 and the disclosure of Shintani, Hao, and Suzuki, the Examiner has failed to explain how such differences would have been obvious to a person of ordinary skill in the art. Accordingly, the Examiner has failed to establish a *prima facie* case of obviousness of claim 38.

Thus, independent claim 38 is patentable over Shintani, Hao, and Suzuki. Dependent claim 40 is also patentable over Shintani, Hao, and Suzuki for at least the same reasons as independent claim 38 from which it depends, and further in view of its own features. Accordingly, Applicants respectfully request that the rejection of claims 38 and 40 be reconsidered and withdrawn.

Other Matters

The Examiner has not set forth any basis for rejecting claim 42. If the Examiner believes that claim 42 should be rejected, Applicants respectfully request that the Examiner provide a detail explanation supporting this belief. Otherwise, Applicants respectfully request that the next Office communication include an explicit indication that claim 42 is allowable.

Added Claims

Claims 43-81 are added. Claim 43 is an independent claim and, with its dependent claims 44-62, distinguishes over the art of record at least by reciting:

> "renaming logic configured to concurrently establish an association between each instruction in a set of instructions concurrently received from the instruction fetch unit and a respective one of the temporary buffers in a selected one of the groups of temporary buffers, wherein a position of each instruction within the set of instructions determines which one of the temporary buffers in the selected group of temporary buffers is associated with that instruction."

Claim 63 is also an independent claim and, with its dependent claims 64-81, distinguishes over the art of record at least by reciting:

> "concurrently establishing an association between each instruction in the set of instructions delivered by the instruction fetch unit and a respective one of the temporary buffers in a selected one of the groups of temporary buffers, wherein a position of each instruction within the set of instructions determines which one of the temporary buffers in the selected group of temporary buffers is associated with that instruction."

Applicants respectfully request that new claims 43-81 be entered, considered, and allowed.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jonathan Tuminaro

Jonathan Tuminaro
Agent for Applicants
Registration No. 61,327

Date: 12/5/07

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

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